DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

PROGRAM STRUCTURE AND SYLLABUS

For

M.TECH (EMBEDDED SYSTEMS)

(Applicable from the Academic Year 2023-24 onwards)

ADITYA COLLEGE OF ENGINEERING & TECHNOLOGY (A)

(An Autonomous Institution)

Approved by AICTE, Affiliated to JNTUK, Accredited by NBA,
Accredited by NAAC A+ Grade with CGPA 3.4
Recognized by UGC under sections 2(f) and 12(B) of UGC act 1956
Aditya Nagar, ADB Road, Surampalem – 533 437, Kakinada District, A.P.
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Ch. Raghu

ADITYA COLLEGE OF ENGINEERING & TECHNOLOGY * SURAMPALEM *

PRINCIPAL
Aditya College of
Engineering & Technology
SURAMPALEM

VISION & MISSION OF THE INSTITUTE

VISION

To induce higher planes of learning by imparting technical education with

- International standards
- Applied research
- Creative Ability
- Value based instruction and to emerge as a premiere institute.

MISSION

Achieving academic excellence by providing globally acceptable technical education by forecasting technology through

- Innovative Research and development
- Industry Institute Interaction
- Empowered Manpower

VISION & MISSION OF THE DEPARTMENT

VISION

To emerge as a center of excellence in education and research.

MISSION

M1: To establish skill and learning centric infrastructure in thrust areas.
M2: To develop Robotics and IOT based infrastructure Laboratories.
M3: To organize events through industry institute collaborations and promote innovation.
M4: To disseminate knowledge through quality teaching learning process.

PROGRAM STRUCTURE

M.Tech. – I Year I Semester

S.No.	Course Code	Category	Title	L/D	T	P	Credits
1	232EM1T01	PCC	Embedded System Design	3	0	0	3
2	232EM1T02	PCC	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3
3	---	PEC	Professional Elective – I	3	0	0	3
4	---	PEC	Professional Elective – II	3	0	0	3
5	232HS1T01	HSMC	Research methodology and IPR	2	0	0	2
6	232EM1L01	PCC	Embedded System Design Lab (using Embedded-C)	0	0	4	2
7	232EM1L02	PCC	Microcontrollers and Programmable Digital Signal Processors Lab	0	0	4	2
8	---	MC	Audit course – I	2	0	0	0
Total				**16**	**0**	**8**	**18**

M.Tech. – I Year II Semester

S.No.	Course Code	Category	Title	L/D	T	P	Credits
1	232EM2T03	PCC	Digital System Design	3	0	0	3
2	232EM2T04	PCC	Real Time Operating Systems	3	0	0	3
3	---	PEC	Professional Elective -III	3	0	0	3
4	---	PEC	Professional Elective - IV	3	0	0	3
5	232EM2L03	PCC	Real Time Operating Systems Lab	0	0	4	2
6	232EM2L04	PCC	Digital System Design Lab	0	0	4	2
7	232EM2P01	PROJ	Mini Project with Seminar	0	0	4	2
8	---	MC	Audit Course – II	2	0	0	0
Total				**14**	**0**	**12**	**18**

BSC – Basic Science Courses
PCC – Professional Core Courses
HSMC – Humanities and Social Sciences including Management Courses
PEC – Professional Elective Courses
PROJ – Project
MC – Mandatory Courses
OEC – Open Elective Courses

Audit Course – I and Audit Course – II has to be chosen from the following list of courses.

S.No.	Course Code		Name of the Course
	I Semester	II Semester	
1	232MC1A01	232MC2A01	English for Research Paper Writing
2	232MC1A02	232MC2A02	Disaster Management
3	232MC1A03	232MC2A03	Sanskrit for Technical Knowledge
4	232MC1A04	232MC2A04	Value Education
5	232MC1A05	232MC2A05	Constitution of India
6	232MC1A06	232MC2A06	Pedagogy Studies
7	232MC1A07	232MC2A07	Stress Management by Yoga
8	232MC1A08	232MC2A08	Personality Development through Life Enlightenment Skills

Professional Elective – I (I Semester)		
S.No	Course Code	Name of the Course
1	232EM1E01	Digital Signal and Image Processing
2	232EM1E02	Parallel Processing
3	232EM1E03	VLSI signal processing

Professional Elective – II (I Semester)		
S.No	Course Code	Name of the Course
1	232EM1E04	Programming Languages for Embedded Systems
2	232EM1E05	System Design with Embedded Linux
3	232EM1E06	CAD for Digital System

Professional Elective – III (II Semester)		
S.No	Course Code	Name of the Course
1	232EM2E07	Memory Architectures
2	232EM2E08	SoC Design
3	232EM2E09	Sensors and Actuators

Professional Elective – IV (II Semester)		
S.No	Course Code	Name of the Course
1	232EM2E10	Communication Buses and Interfaces
2	232EM2E11	Network Security and Cryptography
3	232EM2E12	Physical design automation

EMBEDDED SYSTEM DESIGN

Semester: I	**L**	**T**	**P**	**C**
Course code: 232EM1T01	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To impart the knowledge on Embedded system design concepts.
COB 2:	To facilitate the students to gain knowledge about the basic functions ofembedded system components such as memories, I/O components, Buses.
COB 3:	To facilitate the knowledge about hardware and software tools, device drivers for embedded industry
COB 4:	To train the students to design systems, test and critically evaluate embedded solutions to real world situations
COB 5:	To illustrate the case studies of different processors for approaching to design the real time embedded systems.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Apply processor based embedded system design concepts to develop anembedded system.
CO 2:	Analyze the hardware components, processor performance of anembedded system design.
CO 3:	Make use of operating systems and embedded programming languagesto develop a real-time system.
CO 4:	Utilize modern development tools, CAD tools for integrating softwareand hardware components in embedded system designs.
CO 5:	Develop an embedded system by understanding the various processorarchitecture case studies along with its applications.

UNIT-I:

Introduction to Embedded Systems:

An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

UNIT-II:

Embedded Hardware:

Embedded hardware building blocks, Embedded Processors–ISA architecture models, Internal processor design, processor performance, Board Memory–ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance.

Embedded board Input/output–Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses–Bus arbitration and timing, integrating the Bus with other board components, Bus performance.

UNIT-III:

Embedded Software:

Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples.
Embedded operating systems–Multitasking and process Management, Memory Management,I/O and file system management, OS standards example–POSIX, OS performance guidelines,Board support packages, Middleware and Application Software–Middleware, Middleware examples, Application layer software examples.

UNIT-IV:

Embedded System Design, Development, Implementation and Testing:

Embedded system design and development life cycle model, creating an embedded system architecture, introduction to embedded software development process and tools-Host and Target machines, linking and locating software, getting embedded software into the target system, issues in Hardware-Software design and co-design.
Implementing the design-The main software utility tool, CAD and the hardware, Translation tools, debugging tools, testing on host machine, simulators, Laboratory tools, System Boot- Up.

UNIT-V:

Embedded System Design-Case Studies:

Case studies-Processor design approach of an embedded system–Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform-Respective Processorarchitectures should be taken into consideration while designing an Embedded System.

Text Books:

1. Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers, Tammy Noergaard, Elsevier(Singapore) Pvt. Ltd. Publications,2005.
2. Embedded system Design: A Unified Hardware/Software Introduction, Frank Vahid,Tony D. Givargis, John Wily & Sons Inc, 2002.
3. Introduction to Embedded Systems, Shibu K.V, Mc Graw Hill.

Reference Books:

1. Embedded System Design, Peter Marwedel, Science Publishers, 2007.
2. Embedded System Design, Arnold S Burger, CMP.
3. Embedded Systems: Architecture, Programming and Design, Rajkamal, TMH.

Web Links:

1. https://www.tutorialspoint.com/embedded_systems/
2. http://nptel.ac.in/courses/106105159/
3. http://www.nptelvideos.in/2012/11/embedded-systems.html
4. http://www.dauniv.ac.in/Embedded_Sys.php
5. https://sites.google.com/site/embeddedsystemddr/ppt

MICRO CONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Semester: I	L	T	P	C
Course code: 232EM1T02	3	0	0	3

Course Objectives:

COB 1:	To understand ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
COB 2:	To compare various ARM processor core based SoC with several features/ peripherals based on requirements of embedded applications.
COB 3:	To be able to identify and characterize architecture of Programmable DSP Processors.
COB 4:	To learn different types of Programmable DSP Processors.
COB 5:	To develop small applications by utilizing the ARM processor core and DSP processor based platform.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Develop the moderate complex programs for embedded applications.
CO 2:	Compare the different ARM processor core based SoC with several features/ peripherals based on requirements of embedded applications.
CO 3:	Analyze the architectures in Programmable DSP processors.
CO 4:	Distinguish the different types of TMS320C6000 family.
CO 5:	Develop digital signal processing applications using code composer studio.

UNIT-I:
ARM Cortex-M3 processor: Applications, Programming model– Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers, Pipeline, Bus Interfaces.

UNIT-II:
Exceptions, Types, Priority, Vector Tables Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

UNIT-III:
LPC17xx microcontroller-Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT-IV:
Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TIDSP processor family.

UNIT-V:

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for applicationdevelopment for digital signal processing.

Text Books:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition.
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture,Programming and Applications", TMH, 2nd Edition.
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.

Reference Books:

1. Steve furber, "ARM System-on-Chip Architecture", Pearson Education.
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley.
3. Technical references and user manuals on.

Web Link:

1. www.arm.com.

DIGITAL SIGNAL AND IMAGE PROCESSING

(Professional Elective – I)

Semester: I	**L**	**T**	**P**	**C**
Course code: 232EM1E01	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To enable the students to know the fundamentals of discrete-time signals and systems in various domains.
COB 2:	To enable the students to learn the concepts of the digital filter design.
COB 3:	To make the students to understand the basics of image sampling, quantization and image transforms.
COB 4:	To enable the students to learn the concepts of image enhancement, image restoration and image segmentation.
COB 5:	To make the students to know the various methods involved in image compression and fundamentals in color image processing.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Analyse discrete-time signals and systems in various domains (i.eTime, Z and Fourier).
CO 2:	Design the digital filters (both IIR and FIR) from the givenspecifications
CO 3:	Analyse the quantization effects in digital filters and understand thebasics of image sampling, quantization and image transforms.
CO 4:	Understand the concepts of image enhancement, image restoration andimage segmentation.
CO 5:	Illustrate the various methods involved in image compression andfundamentals in color image processing.

UNIT-I:

Review of Discrete Time signals and systems. Characterization in time, Z and Fourierdomain. Fast Fourier Transform using Decimation in Time (DIT) and Decimation in Frequency (DIF) Algorithms.

UNIT-II:

IIR Digital Filters: Introduction, Analog filter approximations – Butter worth and Chebyshev. Design of IIR Digital filters from analog filters using Impulse Invariance, Bilinear Transformation methods.

FIR Digital Filters: Introduction, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR & FIR filters.

UNIT-III:

Analysis of Finite Word length Effects: The Quantization Process and Errors, Quantization of Fixed-Point Numbers, Quantization of Floating-Point Numbers, Analysis of Coefficient Quantization effects.

Introduction to Digital Image Processing: Introduction, components in image processing system, Applications of Digital image processing, Image sensing and acquisition, Image sampling, Quantization, Basic Relationships between pixels, Image Transforms: 2D-DFT, DCT, Haar Transform.

UNIT-IV:

Image Enhancement: Intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, the basics of filtering in the frequency domain, image smoothing using frequency domain filters, Image Sharpening using frequency domain filters, Selective filtering.

Image Restoration: Introduction, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position – Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.

Image Segmentation: Fundamentals, point, line, edge detection, thresholding, region based segmentation.

UNIT-V:

Image Compression: Fundamentals, Basic compression methods: Huffman coding, Arithmetic coding, Run-Length coding, Block Transform coding, Predictive coding, Wavelet coding.

Color Image Processing: color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color, noise in color images, color image compression.

Text Books:

1. Digital Signal Processing, Principles, Algorithms, and Applications: John
2. G. Proakis, Dimitris G. Manolakis, Pearson Education/PHI, 2007.
3. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006.
4. Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", PearsonEducation, 2011.
5. S. Jayaraman, S. Esakkirajan, T. Veerakumar, "Digital Image Processing",McGrawHill Publishers, 2009.

Reference Books:

1. Digital Signal Processing: Andreas Antoniou, TATA McGraw Hill, 2006.
2. Digital Signal Processing: MH Hayes, Schaum"s Outlines, TATA Mc-Graw Hill, 2007.
3. Anil K. Jain, "Fundamentals of Digital Image Processing," Prentice Hall of India, 2012.

Web Links:

1. https://www.dsprelated.com
2. http://www.dspguide.com
3. http://www.imageprocessingplace.com
4. https://nptel.ac.in/courses/117105079
5. https://imagingbook.com/links

PARALLEL PROCESSING

(Professional Elective – I)

Semester: I	L	T	P	C
Course code: 232EM1E02	3	0	0	3

Course Objectives:

COB 1:	To make the students aware of Parallel Processing and Pipelining operations.
COB 2:	To demonstrate students about Pipelining principles and advanced techniques
COB 3:	To explain different VLIW processor architectures.
COB 4:	To interpret Multithreaded Architecture with the help of multithreading principle
COB 5:	To impart knowledge about Parallel Programming Techniques.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Illustrate the Performance analysis of Parallel Processing and Pipeliningoperation.
CO 2:	Classify pipelining processors with the help of pipelining principleknowledge.
CO 3:	Make use of VLIW processor architecture knowledge to develop newprocessor models.
CO 4:	Develop solutions for issues in multithreaded processor architectures.
CO 5:	Compose Customizing applications on parallel processing platformsusing Parallel Programming Techniques.

UNIT-I:
Overview of Parallel Processing and Pipelining, Performance analysis, Scalability.

UNIT-II:
Principles and implementation of Pipelining, Classification of pipelining processors. Advanced pipelining techniques, Software pipelining.

UNIT-III:
VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA. Vector and Array Processor, FFT Multiprocessor Architecture.

UNIT-IV:
Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

UNIT-V:
Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms.

Text Books:

1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition.
2. Kai Hwang, "Advanced Computer Architecture", TMH.
3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.

Reference Books:

1. William Stallings, "Computer Organization and Architecture, Designing forperformance" Prentice Hall, Sixth edition.
2. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing", MGH.
3. David Harris and Sarah Harris, "Digital Design and Computer Architecture",Morgan.

VLSI SIGNAL PROCESSING

(Professional Elective – I)

Semester: I	L	T	P	C
Course code: 232EM1E03	3	0	0	3

Course Objectives:

COB 1:	To enable the students to learn about the concept of pipelining and parallel processing in VLSI.
COB 2:	To enable the students to identify applications for unfolding algorithm.
COB 3:	To make the students to understand the analysis of VLSI system withhigh speed and low power.
COB 4:	To equip the students with knowledge of Systolic Design for Space Representations containing Delays.
COB 5:	To make the students to understand the concept of Power Reduction and Estimation techniques in VLSI signal processing.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Explain parallel and pipelining processing techniques.
CO 2:	Identify applications for unfolding algorithm
CO 3:	Analyse Systolic Design for Space Representations containing Delays
CO 4:	Explain Cook-Toom Algorithm, Fast Convolution algorithm by Inspection method.
CO 5:	Analyse Power Reduction techniques and Power Estimation techniques.

UNIT-I:

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT–II:

Folding and Unfolding: Folding-Introduction. Folding Transform, register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems. Unfolding-Introduction. An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT-III:

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2DSystolicArray Design, Systolic Design for Space Representations contain Delays.

UNIT-IV:

Fast Convolution: Introduction–Cook-Toom Algorithm–Wino gard algorithm–Iterated Convolution– Cyclic Convolution– Design of Fast Convolution algorithm by Inspection.

UNIT-V:

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design. Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches.

Text Books:

1. KeshabK. Parthi [A1], VLSI Digital signal processing systems, design and Implementation [A2], Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994.
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.

PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEMS

(Professional Elective – II)

	L	T	P	C
Semester: I				
Course code: 232EM1E04	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To understand programming concepts of Embedded C.
COB 2:	To study various programming techniques in object-oriented programming.
COB 3:	To be able to understand the concepts of C++ programming.
COB 4:	To learn different types of overloading and inheritance.
COB 5:	To describe the different templates and scripting languages.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Develop the moderate complex programs in embedded C.
CO 2:	Compare the different programming techniques in object-oriented programming.
CO 3:	Analyze the algorithm in C++.
CO 4:	Distinguish the different types of overloading & Inheritance.
CO 5:	Understand the templates and scripting languages.

UNIT-I:

Embedded "C" Programming: Bitwise operations, Dynamic memory allocation, OS services. Linked stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Embedded Software Development Cycle and Methods (Waterfall, Agile).

UNIT-II:

Object Oriented Programming: Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism.

UNIT-III:

CPP Programming: "cin", "cout", formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, „this" pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT-IV:

Overloading and Inheritance:

Need of operator overloading, overloading the assignment, Overloading using friends, type conversions, single inheritance, base and derived classes, friend Classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, Polymorphism, virtual functions.

UNIT-V:

Templates:

Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.

Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

Text Books:

1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008.
2. Randal L. Schwartz, "Learning Perl", O"Reilly Publications, 6th Edition 2011.

Reference Books:

1. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002.
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company,1999.
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", JohnWilley & Sons, 2005 Kaufmann.

SYSTEM DESIGN WITH EMBEDDED LINUX

(Professional Elective – II)

Semester: I	L	T	P	C
Course code: 232EM1E05	3	0	0	3

Course Objectives:

COB 1:	To compare Embedded Linux, desktop Linux and Embedded Linux distributions.
COB 2:	To explain embedded Linux architecture and micro kernel architecture.
COB 3:	To choose embedded drivers for typical embedded application.
COB 4:	To analyse application porting and operating system porting.
COB 5:	To be able to write and debug applications and drivers in embedded Linux.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Compare Embedded Linux, desktop Linux and Embedded Linuxdistributions.
CO 2:	Explain embedded Linux architecture and micro kernel architecture.
CO 3:	Choose embedded drivers for typical embedded application.
CO 4:	Analyse application porting and operating system porting.
CO 5:	Write and debug applications and drivers in embedded Linux.

UNIT-I:

Embedded Linux, Vendor Independence, Time to Market, Varied Hardware Support, Open Source, Standards (POSIX®) Compliance, Embedded Linux Versus Desktop Linux, Embedded Linux Distributions, Blue Cat Linux, Cadenux, Denx, Embedded Debian (Emdebian), EL in OS (SYSGO), Metrowerks, Monta Vista Linux, RT Linux Pro, Time Sys Linux.

UNIT-II:

Embedded Linux Architecture, Real-Time Executive, Monolithic Kernels, Microkernel Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence, Boot Loader Phase, Kernel Start-Up, User Space Initialization.

UNIT-III:

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules.

UNIT-IV:

Porting Applications, Architectural Comparison, Application Porting Roadmap, Programming with threads, Operating System Porting Layer (OSPL), Kernel API Driver, Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux.

UNIT-V:

Building and Debugging:

Kernel, Building the Kernel, Building Applications, Building the Root File System, Integrated

Development Environment, Debugging Virtual Memory Problems, Kernel Debuggers, Root file system Embedded Graphics. Graphics System, Linux Desktop Graphics, Embedded Linux Graphics, Embedded Linux Graphics Driver, Windowing Environments, Toolkits, and Applications, Case study of uClinux

Text Books:

1. Karim Yaghmour, "Building Embededd Linux Systems", O'Reilly & Associates.
2. P Raghvan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design and Development", Auerbach Publications

Reference Books:

1. Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach",Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, "Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014.

CAD FOR DIGITAL SYSTEM

(Professional Elective – II)

Semester: I	L	T	P	C
Course code: 232EM1E06	3	0	0	3

Course Objectives:

COB 1:	To understand the fundamentals of CAD tools for modeling, design, test and verification of VLSI systems.
COB 2:	To study various phases of CAD, including simulation, physical design, test and verification.
COB 3:	To be able to demonstrate the knowledge of computational algorithms and tools for CAD.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Explain fundamentals of CAD tools for modeling, design, test and verification of VLSI systems.
CO 2:	Experiment with various phases of CAD, including simulation, physical design, test and verification.
CO 3:	Demonstrate knowledge of computational algorithms and tools for CAD.

UNIT-I:

Introduction to VLSI Methodologies: Design and Fabrication of VLSI Devices, Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules Layout of Basic Devices, Fabrication Process and its Impact on Physical Design, Scaling Methods , Status of Fabrication Process, Issues related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development.

UNIT-II:

VLSI design automation tools: Data Structures and Basic Algorithms, Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, graph theory and Computational complexity, tractable and intractable problems.

UNIT-III:

General purpose methods for combinational optimization-Partitioning: Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithms, Simulated Annealing Simulated Evolution, Other Partitioning Algorithms Performance Driven Partitioning.
Floor planning: Chip planning, Pin Assignment, Integrated Approach.
Placement: Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Performance Driven Placement.
Routing: Global Routing, Problem Formulation, Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms. Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing.

UNIT-IV:
Simulation: Gate-level Modeling and Simulation, Switch-level Modeling and Simulation, **Logic Synthesis and Verification:** Introduction to Combinational Logic Synthesis, Binarydecision Diagrams, Two-level Logic Synthesis,
High-level Synthesis: Hardware Models for High level Synthesis, Internal Representation ofthe Input Algorithm, Allocation, Assignment and Scheduling.

UNIT-V:
MCMs-VHDL-Verilog-implementation of simple circuits using VHDL.

Text Books:
1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".
2. S.H. Gerez, "Algorithms for VLSI Design Automation.

RESEARCH METHODOLOGY AND IPR

Semester: I	L	T	P	C
Course code: 232HS1T01	2	0	0	2

Course Objectives:

COB 1:	To demonstrate the identification of the research problems.
COB 2:	To make the awareness on the literature studies, plagiarism and ethics.
COB 3:	To train the knowledge on technical writing.
COB 4:	To analyze the nature of intellectual property rights and new developments
COB 5:	To facilitate the need of the patent rights.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Understand research problem formulation.
CO 2:	Analyze research related information.
CO 3:	Demonstrate research ethics
CO 4:	Explain the today's world is controlled by Computer, InformationTechnology, but tomorrow world will be ruled by ideas, concept, and creativity.
CO 5:	Discuss that when IPR would take such important place in growth ofindividuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students ingeneral & engineering in particular.
CO 6:	Understand that IPR protection provides an incentive to inventors forfurther research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-III:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-IV:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT-V:

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPRand IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction forscience & engineering students".
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction".
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide forbeginners".

References:

1. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.
2. Mayall, "Industrial Design", McGraw Hill, 1992.
3. Niebel, "Product Design", McGraw Hill, 1974.
4. Asimov, "Introduction to Design", Prentice Hall, 1962.
5. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
6. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008.

Web Links:

1. https://www.wipo.int › documents › ip_innovation_development_fulltext
2. https://www.wipo.int › patent-law › developments › research
3. https://www.cencenelec.eu › research › innovation › IPR › Pages

EMBEDDED SYSTEM DESIGN LAB

Semester: I	**L**	**T**	**P**	**C**
Course code: 232EM1L01	**0**	**0**	**4**	**2**

Course Objectives:

COB 1:	To prepare the students to write the C-programs for various embedded applications.
COB 2:	To support the students to develop the algorithms, flow diagrams, source code and perform the compilation, execution on hardware.
COB 3:	To drive the students to implement small programs to solve well-defined problems on an embedded platform.
COB 4:	To motivate the students to analyse the problem specifications for different embedded system applications.
COB 5:	To impart the design aspects of hardware and software for small digital systems involving microcontrollers.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Outline the key concepts of embedded systems IO, timers, interruptsand interaction with peripheral devices.
CO 2:	Develop the simple application codes by using embedded C.
CO 3:	Analyse the different peripherals interfaces with microcontrollers or ARM processors.
CO 4:	Determine the source code for embedded system according to theapplication with different tools.
CO 5:	Build the application code into Micro controllers or any ARMprocessor developer kits with different tools.

List of Experiments:

1. Write a simple program to print "Hello World"
2. Write a simple program to show a delay
3. Write a loop application to copy values from P1 to P2.
4. Write a C program for counting the no of times that a switch is pressed & released.
5. Write a simple program to create a portable hardware delay.
6. Write a C program to test loop time outs.
7. Write a C program to test hardware based timeouts loops.
8. Illustrate the use of port header file (PORT M) using an interface consisting of akeyword and Liquid crystal display.
9. Develop a simple EOS showing traffic light sequencing.
10. Write a program to display elapsed time over RS-232 Link.
11. Write a program to drive SEOS Using Timer 0.
12. Develop software for milk pasteurization system.
13. Develop & implement a program for intruder alarm system

Lab Requirements:

Software:

1. Keil Micro-vision IDE or Eclipse IDE for C and C++ (YAGARTO Eclipse IDE).
2. LINUX Environment for the compilation using Eclipse IDE & Java with latestversion.

Hardware:

1. The development kits of 8051/PIC Micro controllers or any ARM processor.

Reference Books:

1. Embedded C, Michael J. Pont, Pearson Education, 2nd Edition, 2008.
2. Embedded C Programming: Techniques and Applications of C and PIC MCUS, Newnes;1st edition (October 3, 2014).

MICRO CONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB

Semester: I	L	T	P	C
Course code: 232EM1L02	0	0	4	2

Course Objectives:

COB 1:	To prepare the students to write the Embedded C-programs for ARM Cortex M3 processor.
COB 2:	To support the students to develop the algorithms, flow diagrams, source code and perform the compilation, execution on Cortex M3 developmentboards.
COB 3:	To drive the students to implement and solve well-defined problems on an embedded platform.
COB 4:	To prepare the students to write the Embedded C-programs for DSPC6713 processor.
COB 5:	To impart the design aspects of hardware and software for small digital systems involving microcontrollers and DSPs.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Utilize, Install and configure the tool sets for developing applications based on ARM processor. Core SoC and DSP processor.
CO 2:	Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 development boards.
CO 3:	Develop prototype codes using commonly available on and off chip peripherals on the DSP development boards.
CO 4:	Build the application codes into ARM Cortex M3 processor with different tools.
CO 5:	Build the application codes into DSP C6713 processor with different tools.

List of Experiments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU Tool chain.

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using CodeComposer Studio (CCS).

1. To develop an assembly code and C code to compute Euclidian distance betweenany two Points.
2. To develop assembly code and study the impact of parallel, serial and mixed execution.
3. To develop assembly and C code for implementation of convolution operation.
4. To design and implement filters in C to enhance the features of given input sequence/ sign.

Lab Requirements:Software:

1. Keil Micro-vision IDE or Eclipse IDE for C and C++ (YAGARTO Eclipse IDE).
2. LINUX Environment for the compilation using Eclipse IDE & Java with latestversion.
3. Proteus 7 Simulator.
4. Code Composer Studio (CCS).

Hardware:

1. ARM Cortex-M3 development boards and using GNU Tool chain.
2. DSP C6713 evaluation kits.

Web Links:

1. http://infocenter.arm.com/help/topic/com.arm.doc.ddi0337e/DDI0337E_cortex_m3_r1p1_trm.pdf.
2. https://www.st.com/content/ccc/resource/technical/document/programming_manual/5b/ca/8d/83/56/7f/40/08/CD00228163.pdf/files/CD00228163.pdf/jcr:content/translations/en.CD00228163.pdf

DIGITAL SYSTEM DESIGN

Semester: II	**L**	**T**	**P**	**C**
Course code: 232EM2T03	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To make the students to aware of different algorithms for minimizing the complexity of digital system design.
COB 2:	To demonstrate the students about PLA design aspects, IISc & COMPACT algorithms with suitable examples.
COB 3:	To impart the knowledge on SM charts, design aspects of ROM, PAL and digital circuit design approach using CPLDs, FPGAs and ASICS.
COB 4:	To impart the knowledge about Fault Modeling, Test Patten generation and different methods for fault diagnosis of Combinational circuits.
COB 5:	To impart the knowledge about fault diagnosis methods of Sequential circuits.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Examine CAMP Algorithms for minimizing the complexity of digitalsystem design.
CO 2:	Simplify digital circuits using PLA minimization algorithm (IIScalgorithm) and PLA folding algorithm.
CO 3:	Construct digital circuits using CPLDs, FPGAs and ASICs.
CO 4:	Analyze the functionality of combinational circuits using differentfault diagnosis & test methods.
CO 5:	Analyze the testing aspects and fault diagnosis methods of sequential circuits.

UNIT-I:

Minimization Procedures and CAMP Algorithm:

Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMPI algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II:

PLA Design, Minimization and Folding Algorithms:

Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT-III:

Design of Large Scale Digital Systems:

Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control UNIT design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV:

Fault Diagnosis in Combinational Circuits:

Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Pathsensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, PLA test generation, DFT schemes, built in self-test. Fault tolerance techniques

UNIT-V:

Fault Diagnosis in Sequential Circuits:

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Hamming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

Text Books:

1. Logic Design Theory, N. N. Biswas, PHI.
2. Switching and Finite Automata Theory, Z. Kohavi, TMH, 2nd Edition, 2001.

Reference Books:

1. Fundamentals of Logic Design, Charles H. Roth, Cengage Learning, 5thEdition.
2. Digital Systems Testing and Testable Design, Miron Abramovici, Melvin A.
3. Digital Logic Applications and Design, John M Yarbrough, Thomson Learning, 2001.

Web Links:

1. https://www.scribd.com/document/1935815/NR-311901-Digital-Systems-Design
2. https://www.slideshare.net/yayavaram/pla-minimization-testing
3. https://www.elsevier.com/.../digital-systems-design...fpgas...cplds/.../978-0-7506-8397
4. www.donnamaie.com/Advanced.../Advance%20Logic%20Chap%2012-typed. pdf

REAL TIME OPERATING SYSTEMS

Semester: II	L	T	P	C
Course code: 232EM2T04	3	0	0	3

Course Objectives:

COB 1:	To impart basic designs knowledge on Real time operating system environment.
COB 2:	To enable the students to understand functions and types of Real time operating systems for embedded systems.
COB 3:	To demonstrate the students about different issues involved in Real time operating systems.
COB 4:	To enable the students to learn about different memory management techniques involved in embedded systems.
COB 5:	To enable the students to interpret the concepts of synchronization.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Summarize basic concept of services and tasks in RTOS.
CO 2:	Explain basic semaphore operations and message queues of RTOS.
CO 3:	Explain different interrupts and timer services for embedded applications.
CO 4:	Construct hardware memory management, function of designconsideration for embedded applications.
CO 5:	Analyse synchronization methods and design problems in RTOS.

UNIT-I:

Introduction to Real-Time Operating Systems: Defining RTOS, The scheduler, Kernel Objects and services, Key characteristics of an RTOS.

Task-Defining a Task, Task States and Scheduling, Typical Task Operations, Typical Task Structure, Synchronization, Communication and Concurrency.

UNIT-II:

Semaphores: Defining Semaphores, Typical Semaphore Operations, Typical Semaphore Use

Message Queues: Defining Message Queues, Message Queue States, Message Queue Content, Message Queue Storage, Typical Message Queue Operations, Typical Message Queue Use, Pipes, Event Registers, Signals and condition Variables.

UNIT-III:

Exceptions and Interrupts: Exceptions and Interrupts, Applications of Exceptions andInterrupts, Closer look at exceptions and interrupts, processing general Exceptions, Nature of Spurious Interrupts.

Timer and Timer Services: Real-Time clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routines.

I/O Subsystems-I/O concepts, I/O subsystems.

UNIT-IV:

Memory Management: Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory management in Embedded Systems, Blocking VS. Non-Blocking Memory Functions, Hardware Memory Management Units.

Modularizing an application for concurrency: An outside-in approach to decompose Applications, Guidelines and Recommendations for Identifying Concurrency, Schedule ability Analysis.

UNIT-V:

Synchronization and Communication: Synchronization, Communication, Resource synchronization Methods, Critical section, Common practical design patterns, Specific Solution Design Patterns,

Common Design Problems: Resource Classification, Deadlocks, Priority Inversion.

Text Books:

1. "Real-Time Concepts for Embedded Systems", Qing Li, Caroline Yao, CMP Books,2003.
2. Embedded/Real-Time Systems, Dr. K.V.K.K. Prasad Dream Tech Publications, Blackpad book.
3. Embedded Systems-Architecture, Programming and Design, Raj Kamal, TataMcGraw Hill Publications, 2nd Edition, 2008.

Reference Books:

1. Real-Time Systems: Scheduling, Analysis and Verification", Albert Cheng, "WileyInter science, 2002.
2. "Real-Time Systems: Design Principles for Distributed Embedded Applications",Hermann Kopetz, Kluwer, 1997.
3. "Hand book of Real-Time Systems", Insup Lee, Joseph Leung, Sang Son Chapman,Hall Krishna and Kang G Shin, 2001, 2008.
4. "Real-Time Systems", McGraw Hill.
5. Real Time Concepts for Embedded Systems, Qing Li, Elsevier, 2011.

Web Links:

1. https://exploreembedded.com/wiki/RTOS_Basics
2. https://www.highintegritysystems.com
3. www.intervalzero.com/RTOS

MEMORY ARCHITECTURES

(Professional Elective – III)

	L	T	P	C
Semester: II				
Course code: 232EM2E07	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To make the students understand the various SRAM architectures with respect to MOS and Bipolar technologies.
COB 2:	To make the students study and understand about the various DRAM architectures and memory controllers.
COB 3:	To impart the knowledge on the non-volatile memories based on various types of ROM architectures.
COB 4:	To make the students study about the various radiation effects and design issues on semiconductor memory.
COB 5:	To make the students aware of the advanced memory technologies and memory packing technologies.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Select architecture and design semiconductor memory circuits and subsystems.
CO 2:	Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
CO 3:	Know how the state-of-the-art memory chip design.

UNIT-I:

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT-II:

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

UNIT-III:

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT-IV:

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques, Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

UNIT-V:

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing andReliability Issues,

Text Books:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Inter science.
2. Kiyooltoh, "VLSI memory chip design", Springer International Edition.

Reference Books:

1. Ashok K Sharma, "Semiconductor Memories: Technology, Testing and Reliability, PHI.

SoC DESIGN

(Professional Elective – III)

	L	T	P	C
Semester: II				
Course code: 232EM2E08	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To get fundamental concepts of system-on-chip approach of designing complex VLSI systems and challenges.
COB 2:	To understand Application Specific Integrated Circuits design flow.
COB 3:	To get familiar with No Instruction Set Computing architecture and different simulation models.
COB 4:	To understand utilization of low power techniques for SoC design.
COB 5:	Demonstrate various simulation methods and synthesis techniques for SoCs.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Compare Sob, SoC and SiP for electronic product in terms of size,cost, performance and reliability.
CO 2:	Analyze different approaches for solving architectural issues of SoC design.
CO 3:	Discuss NISC and use of ADL.
CO 4:	Identify different simulation modes and modelling of reconfigurablesystems.
CO 5:	Appraise low power SoC design.

UNIT-I:

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches forSOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT-II:

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer(NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation- A formal language for specification, compilation and synthesis of embedded processors.

UNIT-III:

Simulation: Different simulation modes behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors. Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT-IV:

Low power SoC design / Digital system: Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock

frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT-V:

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerantdesigns.

Text Books:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures toCMOS.
2. Fabrication", Cambridge University Press, 2008.
3. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006.

Reference Books:

1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R&D Center, 2000.
2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk," Computer System Design: System-on-Chip".

Web Links:

1. https://en.wikipedia.org/wiki/System_on_a_chip
2. https://www.peterindia.net/System-On-ChipLinks.html
3. https://www.ieee-socc.org/
4. http://nptel.ac.in/courses/108102045/10

SENSORS AND ACTUATORS

(Professional Elective – III)

	L	T	P	C
Semester: II				
Course code: 232EM2E09	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To make students to understand basic laws and phenomena for operation of Sensors and Actuators.
COB 2:	To impart the knowledge on analysis, design and development solutions for sensors and actuators.
COB 3:	To enable the students to classify various thermal, radiation and smart sensors available.
COB 4:	To impart the knowledge on various control values of actuators.
COB 5:	To make the students to understand implementation of various Actuators.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Classify various sensors/transducers based on their applications.
CO 2:	Dissect various types of Resistive, Inductive and Capacitive Sensors.
CO 3:	Analyze various approaches, procedures and results related to Thermal and Magnetic sensors.
CO 4:	Examine the radiation sensors based on their characteristics.
CO 5:	Apply Smart Sensors in the field of Communication, Automation and Manufacturing.
CO 6:	Perceive various control values and types of actuators.

UNIT-I:

Sensors / Transducers: Principles – Classification – Parameters – Characteristics – Environmental Parameters (EP) – Characterization.

Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors.

UNIT-II:

Thermal Sensors: Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and RefractiveIndex thermo sensors – Helium Low Temperature Thermometer – Nuclear Thermometer –Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermo emf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz CrystalThermoelectric Sensors – NQR Thermo metry – Spectroscopic Thermometry – NoiseThermometry – Heat Flux Sensors.

Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magneto resistive Sensing – Semiconductor Magneto resistors– Hall Effect and

Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flow meter – Switching Magnetic Sensors SQUID Sensors.

UNIT-III:

Radiation Sensors: Introduction – Basic Characteristics – Types of Photo sensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors.

Electro analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media.

UNIT - IV:

Smart Sensors: Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation

Sensors-Applications: Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring.

UNIT-V:

Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Pressure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators

Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors.

Text Books:

1. D. Patranabis – "Sensors and Transducers" –PHI Learning Private Limited.
2. W. Bolton – "Mechatronics" –Pearson Education Limited.

Reference Books:

1. Sensors and Actuators – D. Patranabis – 2nd Ed., PHI, 2013.

COMMUNICATION BUSSES AND INTERFACES

(Professional Elective – IV)

Semester: II	**L**	**T**	**P**	**C**
Course code: 232EM2E10	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To Study different types of serial buses and their applications.
COB 2:	To analyze architecture of CAN and its applications.
COB 3:	To learn different types of interconnects and their configurations.
COB 4:	To illustrate various types of data transfers and descriptor.
COB 5:	To explain variety of serial communication protocols.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Select a particular serial bus suitable for a particular application.
CO 2:	Apply the knowledge of CAN protocol for real time applications.
CO 3:	Develop APIs for configuration, reading and writing data onto serial bus.
CO 4:	Outline different types of data transfer mechanisms.
CO 5:	Design peripherals that can be interfaced to desired serial bus.

UNIT-I:

Serial Busses- Cables, Serial busses, serial versus parallel. Data and Control Signal- dataframe, data rate, features Limitations and applications of RS232, RS485, I^2C, SPI.

UNIT-II:

CAN: ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Overload frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT-III:

PCIE: Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT-IV:

USB: Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

UNIT-V:

Data streaming Serial Communication Protocol- Serial Front Panel Data Port (SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

Text Books:

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Ports and Ports for Embedded Systems-Jan Axelson, Lakeview Research, 2nd Ed.,

References:

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

NETWORK SECURITY AND CRYPTOGRAPHY

(Professional Elective – IV)

	L	T	P	C
Semester: II				
Course code: 232EM2E11	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To impart basic knowledge on encryption techniques.
COB 2:	To enable the students to understand the concepts of data encryption standards using algorithms.
COB 3:	To impart basic knowledge on Fermat's and Euler's theorems.
COB 4:	To demonstrate the students about the concepts of authentication protocols and digital signature.
COB 5:	To illustrate the students about web design security and fire-wall design principles.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Explain basic concepts of encryption techniques.
CO 2:	Identify and utilize different forms of cryptography techniques.
CO 3:	Illustrate authentication requirements with algorithms.
CO 4:	Apply authentication and security in the network applications.
CO 5:	Compare different types of threats to the system and handle the same.

UNIT–I:

Security & Number Theory

Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security. Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques. Introduction, Fermat"s and Euler"s Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT-II:

Private-Key (Symmetric) Cryptography

Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES),Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT-III:

Public-Key (Asymmetric) Cryptography

RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT-IV:

Authentication:

IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols,

Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

UNIT-V:

System Security:

Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Counter measures, Firewalls, Firewall Design Principles, Trusted Systems.

Text Books:

1. Cryptography and Network Security, Behrouz A. Forouzan and Debdeep Mukhopadhay, Tata McGrawHill, 2010.
2. William Stallings, "Cryptography and Network Security, Principles and Practices",Pearson Education, 3rd Edition.
3. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
4. Cryptography and Network Security: Principles and Practice, William Stallings, William Stallings, Pearson Education, 5th Edition, 2011.

Reference Books:

1. Principles of Network and Systems Administration, Mark Burgess, JohnWiey.
2. Fundamentals of Network Security, Eric Maiwald, (Dreamtech press).
3. Network Security, Private Communication in a Public World, Charlie Kaufman, Radia Perlman and Mike Speciner, Pearson/PHI.
4. Principles of Information Security, Whitman, Thomson.

Web Links:

1. http://www.freeswan.org/freeswan_trees/freeswan-1.5/doc/links.crypto.html
2. https://www.cse.iitb.ac.in/~cs406/Resources.htm
3. http://www.mathaware.org/mam/97/links/security.html
4. http://www.math.stonybrook.edu/~scott/blair/Blair_s_Cryptography_Notes.html
5. http://www.comap.com/highschool/projects/mmow/weblinks_c1_g9_u2.htm
6. http://www.ciphersbyritter.com/LEARNING.HTM#Fundamental
7. http://www.cimt.org.uk/resources/codes/codes_u10_tr.pdf
8. http://williamstallings.com/Extras/Security-Notes/lectures/classical.html

PHYSICAL DESIGN AUTOMATION

(Professional Elective – IV)

	L	T	P	C
Semester: II				
Course code: 232EM2E12	**3**	**0**	**0**	**3**

Course Objectives:

COB 1:	To understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.
COB 2:	To learn the design algorithms to meet the critical design parameters.
COB 3:	To know the layout optimization techniques and map them to the algorithms.
COB 4:	To understand proto-type EDA tools and know how to test its efficacy.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.
CO 2:	Adapt the design algorithms to meet the critical design parameters.
CO 3:	Identify layout optimization techniques and map them to the algorithms.
CO 4:	Develop proto-type EDA tool and test its efficacy.
CO 5:	Analyze the different partitioning algorithms and its evolution.

UNIT-I:

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chipmodules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNIT-II:

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph andComputational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

UNIT-III:

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbor pointers, corner stitching, multi-layer operations.

UNIT-IV:

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

UNIT-V:

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms,

simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition.Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

Web links:

1. https://nptel.ac.in/courses/106105161/
2. https://eecs.wsu.edu/~daehyun/teaching/2014_EE582/
3. http://users.ece.utexas.edu/~dpan/PDA_syllabus.pdf

REAL TIME OPERATING SYSTEMS LAB

Semester: II	L	T	P	C
Course code: 232EM2L03	0	0	4	2

Course Objectives:

COB 1:	To make the students, in writing the programs using Embedded C according tothe Experiment requirements using RTOS on embedded processors.
COB 2:	To prepare the students to develop the algorithms, flow diagrams, source codeand perform the compilation, execution.
COB 3:	To drive the students to implement the embedded system for verification.
COB 4:	To enable the student to interface the peripherals and work with real time environment.
COB 5:	To make the students, to work with recent areas of the embedded system design.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Outline the architectural support of ARM for Real Time Operating Systems with different tools.
CO 2:	Develop the algorithms, flow diagrams, source code and perform the compilation and execution.
CO 3:	Test for ARM-926 developer kits and ARM-Cortex with different tools.
CO 4:	Interpret the data for an embedded system in the real time environment.
CO 5:	Compare the results for optimization of the real time embedded system with existing.

List of Experiments:

Part-I: Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II Experiments on ARM-CORTEX processor using any open source RTOS (Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

1. Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
2. LINUX Environment for the compilation using Eclipse IDE & Java with latestversion.

Hardware:

1. The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
2. Serial Cables, Network Cables and recommended power supply for the board.

Reference Books:

1. An Embedded Software Primer, simon, Pearson Education, 1st Edition 2002.

DIGITAL SYSTEMS DESIGN LAB

Semester: II	**L**	**T**	**P**	**C**
Course code: 232EM2L04	**0**	**0**	**4**	**2**

Course Objectives:

COB 1:	To impart the knowledge on HDL design flow for digital system design.
COB 2:	To make the students to simulate and synthesis the HDL design under given constraints.
COB 3:	To enable the students to make use of various minimization algorithms used in digital system design.
COB 4:	To familiarize the students with the necessary knowledge about the CAD toolsfor design and implementation of given digital systems on FPGA and CPLD devices.

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Utilize the higher order minimization algorithms to minimize the Boolean functions and Programmable Logic Arrays.
CO 2:	Develop the logic to implement ROM, Control unit and data processor.
CO 3:	Apply Industry standard simulator to verify the logical /functional operation.
CO 4:	Analyse the synthesis report in order to meet the given constraints.
CO 5:	Utilize the hardware modules FPGA and CPLD for real time verification.

Systems Design experiments:

- The students are required to design the logic to perform the following experiments using necessary Industry standard simulator to verify the logical /functional operation, perform the analysis with appropriate synthesizer and to verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).
- Consider the suitable switching function and data to implement the required logic if required.
- A student has to do at least 10 Experiments.

List of Experiments:

1. Determination of EPCs using CAMP-I Algorithm.
2. Determination of SPCs using CAMP-I Algorithm.
3. Determination of SCs using CAMP-II Algorithm.
4. PLA minimization algorithm (IISc algorithm).
5. PLA folding algorithm (COMPACT algorithm).
6. ROM design.
7. Control unit and data processor logic design.
8. Digital system design using FPGA.
9. Kohavi algorithm.
10. Hamming experiments.

MINI PROJECT WITH SEMINAR

Semester: II	**L**	**T**	**P**	**C**
Course code: 232EM2P01	**0**	**0**	**4**	**2**

Course Outcomes: At the end of the Course, Student will be able to:

CO 1:	Understand of contemporary / emerging technology for various processes and systems.
CO 2:	Share knowledge effectively in oral and written form and formulate documents.

Syllabus Contents

The students are required to search / gather the material / information on a specific a topic comprehend it and present / discuss in the class.

ENGLISH FOR RESEARCH PAPER WRITING

(Common to all branches)

Semester: I or II	**L**	**T**	**P**	**C**
Course code: 232MC1A01 or 232MC2A01	**2**	**0**	**0**	**0**

Course Objectives:

COB 1:	Understand how to improve the writing skills and level of readability.
COB 2:	Illustrate what to write in each section.
COB 3:	Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission.

Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Skills are needed when skills are needed when Conclusions. writing the Methods, skills needed when writing the Results, writing the Discussion, skills are needed when writing the conclusions.

Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

Text Books:

1. Gold bort R (2006) Writing for Science, Yale University Press (available on Google Books).
2. Day r (2006) How to Write and Publish a Scientific Paper, Cambridge University Press.
3. High man N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. High man's book.
4. Adrian Wall work, English for Writing Research Papers, Springer New York Dordrech Heidelberg London, 2011.

DISASTER MANAGEMENT

(Common to all branches)

Semester: I or II	L	T	P	C
Course code: 232MC1A02 or 232MC2A02	2	0	0	0

Course Objectives:

COB 1:	Demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
COB 2:	Evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
COB 3:	Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
COB 4:	Understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Introduction:
Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem.
Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, DroughtsAnd Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

Disaster Prone Areas in India:
Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics.

Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

Risk Assessment:
Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

Disaster Mitigation:
Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs Of Disaster Mitigation in India.

Text Books:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies" New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences And Reflections",Prentice Hall Of India, New Delhi.
3. Goel S. L., "Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi.

SANSKRIT FOR TECHNICAL KNOWLEDGE

(Common to all branches)

Semester: I or II	**L**	**T**	**P**	**C**
Course code: 232MC1A03 or 232MC2A03	**2**	**0**	**0**	**0**

Course Objectives:

COB 1:	Knowledge in illustrious Sanskrit, the scientific language in the world.
COB 2:	Improve brain functioning.
COB 3:	Develop the logic in mathematics, science & other subjects enhancing the memory power.
COB 4:	Explore the huge knowledge from ancient literature.

Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences.

Order, Introduction of roots, Technical information about Sanskrit Literature.

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics.

Text Books:

1. "Abhyas pustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi.
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication.
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., NewDelhi.

VALUE EDUCATION

(Common to all branches)

Semester: I or II	L	T	P	C
Course code: 232MC1A04 or 232MC2A04	2	0	0	0

Course Objectives:

COB 1:	Understand value of education and self- development.
COB 2:	Explain the need of good values in students.
COB 3:	Developing the overall personality.
COB 4:	Explain the need of character in a student.

Values and self-development: Social values and individual attitudes. Work ethics, Indian vision of humanism, Moral and non- moral valuation. Standards and principles, Value judgments.

Importance of cultivation of values: Sense of duty, Devotion, Self-reliance, Confidence, Concentration. Truthfulness, Cleanliness, Honesty, Humanity. Power of faith, National Unity, Patriotism. Love for nature, Discipline.

Personality and Behavior Development: Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship.
Happiness Vs suffering, love for truth, Aware of self- destructive habits, Association and Cooperation, Doing best for saving nature.

Character and Competence: Holy books vs Blind faith, Self-management and Good health, Science of reincarnation, Equality, Nonviolence, Humility, Role of Women, All religions and same message, Mind your Mind, Self-control, Honesty, Studying effectively.

Text Books:

1. Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi.

CONSTITUTION OF INDIA

(Common to all branches)

	L	T	P	C
Semester: I or II				
Course code: 232MC1A05 or 232MC2A05	**2**	**0**	**0**	**0**

Course Objectives:

COB 1:	Describe the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
COB 2:	Explain the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
COB 3:	Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
COB 4:	Demonstrate the passage of the Hindu Code Bill of 1956.

History of Making of the Indian Constitution: History.Drafting Committee, (Composition & Working).

Philosophy of the Indian Constitution:
Preamble Salient Features.

Contours of Constitutional Rights & Duties:
Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

Organs of Governance:
Parliament Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

Local Administration:
District's Administration head: Role and Importance,
Municipalities: Introduction, Mayor and role of Elected Representative, CE of Municipal Corporation.
Pachayati raj: Introduction, PRI: Zila Pachayat, Elected officials and their roles.
CEO Zila Pachayat: Position and role.
Block level: Organizational Hierarchy (Different departments),
Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

Election Commission:
Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners.
State Election Commission: Role and Functioning, Institute and Bodies for the welfare of

SC/ST/OBC and women.

Text Books:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition,2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015

PEDAGOGY STUDIES

(Common to all branches)

	L	T	P	C
Semester: I or II				
Course code: 232MC1A06 or 232MC2A06	**2**	**0**	**0**	**0**

Course Objectives:

COB 1:	Distinguish the various pedagogical practices are being used by teachers in formal and informal classrooms in developing countries.
COB 2:	Explain the evidence on the effectiveness of various kinds of pedagogical practices, in different conditions.
COB 3:	Discuss the teacher's attitudes and beliefs in line with pedagogic strategies.
COB 4:	Prepare school curriculum and guidance material best support effective pedagogy.
COB 5:	List the research gaps.

Introduction and Methodology:
Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education, Conceptual framework, Research questions, Overview of methodology and Searching.

Thematic overview:
Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries, Curriculum, Teacher education.

Evidence on the effectiveness of pedagogical practices:
Methodology for the in depth stage: quality assessment of included studies, How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change, Strength and nature of the body of evidence for effective pedagogical practices, Pedagogic theory and pedagogical approaches, Teachers" attitudes and beliefs and Pedagogic strategies.

Professional development:
Alignment with classroom practices and follow-up support.Peer support, Support from the head teacher and the community, Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

Research gaps and future directions:
Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Text Books:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools,Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance ofevaluation, Journal of Curriculum Studies, 36 (3): 361-379.

3. A kyeampong K (2003) Teacher training in Ghana - does it count? Multi-siteteacher education research project (MUSTER) country report 1. London: DFID.
4. A kyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching andlearning of basic Maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons inprimary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, learning to read campaign.

Web Link:

1. www.pratham.org/images/resource%20working%20paper%202.pdf.

STRESS MANAGEMENT BY YOGA

(Common to all branches)

Semester: I or II	L	T	P	C
Course code: 232MC1A07 or 232MC2A07	2	0	0	0

Course Objectives:

COB 1:	Develop healthy mind in a healthy body to improve social health.

Definitions of Eight parts of yoga. (Ashtanga):
Yam and Niyam. Do`s and Dont's in life:

i) Ahinsa, satya, astheya, bramhacharya and aparigraha.
ii) Shaucha, santosh, tapa, swadhyay, is hwarpranidhan.

Asan and Pranayam:

1. Various yog poses and their benefits for mind & body.
2. Regularization of breathing techniques and its effects-Types of pranayama.

Text Books:

1. "Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yoga bhyasi Mandal,Nagpur.
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda,Advaita Ashrama (Publication Department), Kolkata.

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

(Common to all branches)

Semester: I or II	L	T	P	C
Course code: 232MC1A08 or 232MC2A08	2	0	0	0

Course Objectives:

COB 1:	Develop his/her personality and achieve the highest goal in life.
COB 2:	Capable of lead the nation and mankind to peace and prosperity.
COB 3:	Develop versatile personality of students.

Neetisatakam-Holistic development of personality

Verses- 19,20,21,22 (wisdom), Verses- 29,31,32 (pride & heroism), Verses- 26,28,63,65 (virtue), Verses- 52,53,59 (dont's), Verses- 71,73,75,78 (do's).

Approach to day to day work and duties, Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48, Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, Chapter 18-Verses 45, 46, 48.

Statements of basic knowledge, Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68, Chapter 12 -Verses 13, 14, 15, 16,17, 18, Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42, Chapter 4-Verses 18, 38,39, Chapter18 – Verses 37,38,63.

Text Books:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

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